to and operatively connected with said [image] light sensor region,

wherein said semiconductor layer has at least one of an electron mobility [15-100] 15-300 cm^2/V sec and a hole mobility [10-100] 10-200 cm^2/V sec.

13. (Amended) The device of claim 9 wherein said semiconductor layer has at least one of an electron mobility in a range from [15 to 100] 15- 300 cm^2/V sec and a hole mobility in a range from [10 to 100] 10-200 cm^2/V sec.

14. (Amended) The device of claim 1 wherein said semiconductor layer has at least one of an electron mobility in a range from [15 to 100] 15-300 cm^2/V sec and a hole mobility in a range from [10 to 100] 10-200 cm^2/V sec.

22. (Amended) A device for reading an image comprising:

a semiconductor layer formed on a substrate, said semiconductor layer comprising an image sensor region and a semiconductor switch region adjacent to and operatively connected with said image sensor region,

wherein said semiconductor layer has at least one of an electron mobility 15-300 cm^2/V sec and a hole mobility 10-200 cm^2/V sec.

27. (Amended) The device of claim 23 wherein said semiconductor layer has at least one of an electron mobility in a range from 15 to 300 cm^2/V sec and a hole mobility in a range from 10 to 200 cm^2/V sec.

28. (Amended) The device of claim 15 wherein said semiconductor layer has at least one of an electron mobility in a range from 15 to 300cm^2/V sec and a hole mobility in a range from 10 to 200 cm^2/V sec.

Please add the following new claims:

31. A semiconductor device comprising:

a substrate;

a blocking layer on said substrate;

first and second semiconductor islands on said blocking layer;

a pair of p-type impurity regions in said first semiconductor island with a first channel region interposed therebetween;

a pair of n-type impurity regions in said second semiconductor island with a second channel region;

a gate insulating film on said first and second semiconductor islands; and

first and second gate electrodes over said first and second channel regions, respectively, with said gate insulating film interposed therebetween,

wherein a Raman spectrum of each of said first and second semiconductor islands exhibits a peak deviated from that which stands for a single crystal of the semiconductor.

32. A device according to claim 31, wherein said blocking layer comprises silicon oxide.

33. A device according to claim 31, wherein said gate insulating film is a silicon oxide film containing fluorine.

34. A device according to claim 31, said p-type impurity regions contain boron.

35. A device according to claim 31, said N-type impurity regions contain phosphorus.

36. A semiconductor device comprising:

a substrate;

a blocking layer on said substrate;

first and second semiconductor islands on said blocking layer;

a pair of p-type impurity regions in said first semiconductor island with a first channel region interposed therebetween;

a pair of n-type impurity regions in said second semiconductor island with a second channel region;

a gate insulating film on said first and second semiconductor islands; and

first and second gate electrodes over said first and second channel regions, respectively, with said gate insulating film interposed therebetween,

wherein said first semiconductor island has a mobility of 10-300 $cm^2/Vsec$ and said second semiconductor island has a mobility of 15-300 $cm^2/Vsec$.

37. A device according to claim 32, wherein said blocking layer comprises silicon oxide.

38. A device according to claim 32, wherein said gate insulating film is a silicon oxide film containing fluorine.

39. A device according to claim 32, said p-type impurity regions contain boron.

40. A device according to claim 32, said N-type impurity regions contain phosphorus.